26. (Currently Amended) The multimedia interface according to claim 23, further comprising a programmable, fast serial interface core to interface to a serial interface standard incorporated on the IC chip.

Sub C1

27. (Previously Added) The multimedia interface according to claim 23, further comprising a programmable CPU interface core incorporated on the IC chip.

28. (Previously Added) The multimedia interface according to claim 23, further comprising a programmable memory interface (PMI) core incorporated on the IC chip.

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29. (Currently Amended) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the I C chip;

a media processor block incorporated on the IC chip; [and]

audio and/or video CODEC incorporated on the IC chip for interfacing to external analog signals; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the audio and/or video CODEC is not in use.

30. (Currently Amended) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; [and]

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing saving when the PLL circuitry is not in use.

31. (Currently Amended) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; [and]

a programmable, fast serial interface core to interface to a serial interface standard incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the serial interface core is not in use.

32. (Currently Amended) Multimedia interface [according to claim 31, wherein:], comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable, fast serial interface core to interface to a serial interface standard [the programmable, fast serial interface core is] incorporated within the reconfigurable logic block.

33. (Currently Amended) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; [and]

a programmable CPU interface core incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the programmable CPU interface core is not in use.

34. (Previously Added) Multimedia interface according to claim 33, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

35. (Currently Amended) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip, the PMI core communicates with off-chip memory and configures it virtually into what is optimal for an application that demands non-standard size memory.

Sub C1

36. (Currently Amended) Multimedia interface according to claim [35] **52**, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

B1

37. (Previously Added) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODECs for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use. (no change)

38. (Currently Amended) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; [and]

audio and/or video CODEC for interfacing to external analog signals incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the audio and/or video CODEC is not in use.

Sub C1

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39. (Currently Amended) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; [and]

phase locked loop (PLL) circuitry incorporated on the IC chip to reduce skew within various blocks within the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the PLL circuitry is not in use.

40. (Currently Amended) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; [and]

a programmable, fast serial interface core to interface to a serial interface standard incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the serial interface core is not in use.

41. (Currently Amended) Signal processing interface [according to claim 40, wherein:], comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable, fast serial interface core to interface to a serial interface standard [the programmable, fast serial interface core is] incorporated within the reconfigurable logic block.

42. (Currently Amended) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; [and]

a programmable CPU interface core incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the programmable CPU interface core is not in use.

Sub C1

43. (Previously Added) Signal processing interface according to claim 42, wherein:

the programmable CPU interface core is incorporated within the reconfigurable logic block.

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44. (Currently Amended) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

a programmable memory interface (PMI) core incorporated on the IC chip, the PMI core communicates with off-chip memory and configures it virtually into what is optimal for an application that demands non-standard size memory.

45. (Currently Amended) Signal processing interface according to claim [44] **58**, wherein:

the programmable memory interface core is incorporated within the reconfigurable logic block.

46. (Previously Added) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

at least one additional core selected from the group consisting of

audio and/or video CODEC for interfacing to external analog signals;

phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip;

a programmable, fast serial interface core;

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a programmable CPU interface core;

a programmable memory interface (PMI) core; and

further comprising power-down circuitry, in combination with one or more of these additional cores, incorporated on the IC chip to provide power and/or processing savings when a given one of the cores is not in use.

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47. (New) The multimedia interface according to claim 23, further comprising a configuration port that allows a user access to the block of reconfigurable logic from off-chip.

48. (New) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the I C chip;

a media processor block incorporated on the IC chip; and

audio and/or video CODEC and an analog interface incorporated on the IC chip, the audio and/or video CODEC communicating, via the analog interface, with external analog signals.

49. (New) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip;

means, incorporated on the IC chip, for reducing skew within various blocks within the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing saving when the means for reducing skew is not in use.

50. (New) The multimedia interface according to claim 31, wherein the serial interface standard is one of USB and IEEE-1394.

51. (New) The multimedia interface according to claim 32, wherein the serial interface standard is one of USB and IEEE-1394.

52. (New) Multimedia interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a media processor block incorporated on the IC chip;

a programmable memory interface (PMI) core incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the PMI core is not in use.

53. (New) The multimedia interface according to claim 37, wherein the media processor has a virtual instruction set capable of implementing a variety of multimedia algorithms.

54. (New) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip; and

audio and/or video CODEC and an analog interface incorporated on the IC chip, the audio and/or video CODEC communicating, via the analog interface, with external analog signals.

55. (New) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip;

means, incorporated on the IC chip, for reducing skew within various blocks within the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing saving when the means for reducing skew is not in use.

56. (New) The signal processing interface according to claim 40, wherein the serial interface standard is one of USB and IEEE-1394.

57. (New) The signal processing interface according to claim 41, wherein the serial communication standard is one of USB and IEEE-1394.

58. (New) Signal processing interface, comprising:

an integrated circuit (IC) chip;

a block of reconfigurable logic incorporated on the IC chip;

a RISC core incorporated on the IC chip;

a programmable memory interface (PMI) core incorporated on the IC chip; and

further comprising power-down circuitry incorporated on the IC chip to provide power and/or processing savings when the PMI core is not in use.